Semi-Reconfigurable Processors for Fast Image Analysis

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March 31, 2011

Summary

- Realtime image analysis
- The IMAP architecture
- IMAP-CE and IMAPCAR
- IMAPCAR2

Realtime image analysis - what is it?

- Transformation and analysis of images in real time
  - Typically, this means 30fps or 60fps
  - At 30fps you have about 33ms to process each frame
- Subset of *realtime image processing*
- Significantly more difficult than transformation only

Realtime image analysis - what is it good for?

- Obstacle detection and avoidance
- Lane following
- Threat detection
- Object identification
- In short: machine vision

Realtime image analysis - the problem

- 30fps image analysis is not cheap
- Embedded processors don't have the power
- GPPs are too expensive and too power-hungry
- ASICs are too inflexible

GPP	General Purpose Processor
ASIC	Application Specific Integrated Circuit

IMAP - the Integrated Memory Array Processor

- Described by Fukushima et al. in 1995
- Designed to quickly and cheaply perform image processing tasks
- 8-bit SIMD RISC architecture
- Intended to act as a coprocessor to a separate CPU

RISC	Reduced Instruction Set Computer
SIMD	Single Instruction Multiple Data

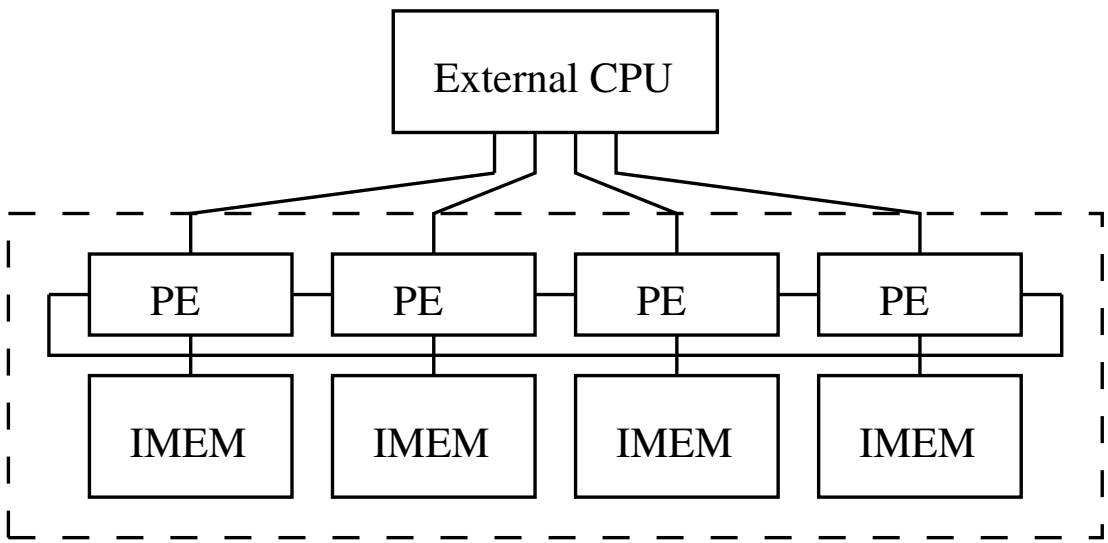
IMAP - Internal Components

- 64 8-bit SIMD PEs
- 2KB of IMEM per PE
- Simple ring network connecting PEs
- Tree network connecting external CPU to PEs

PE	Processing Element - a SIMD miniprocessor
IMEM	Internal Memory

IMAP - Internal Design

- Each PE can only directly access its own registers and IMEM
- Ring network lets PEs transfer data to registers of adjacent PEs



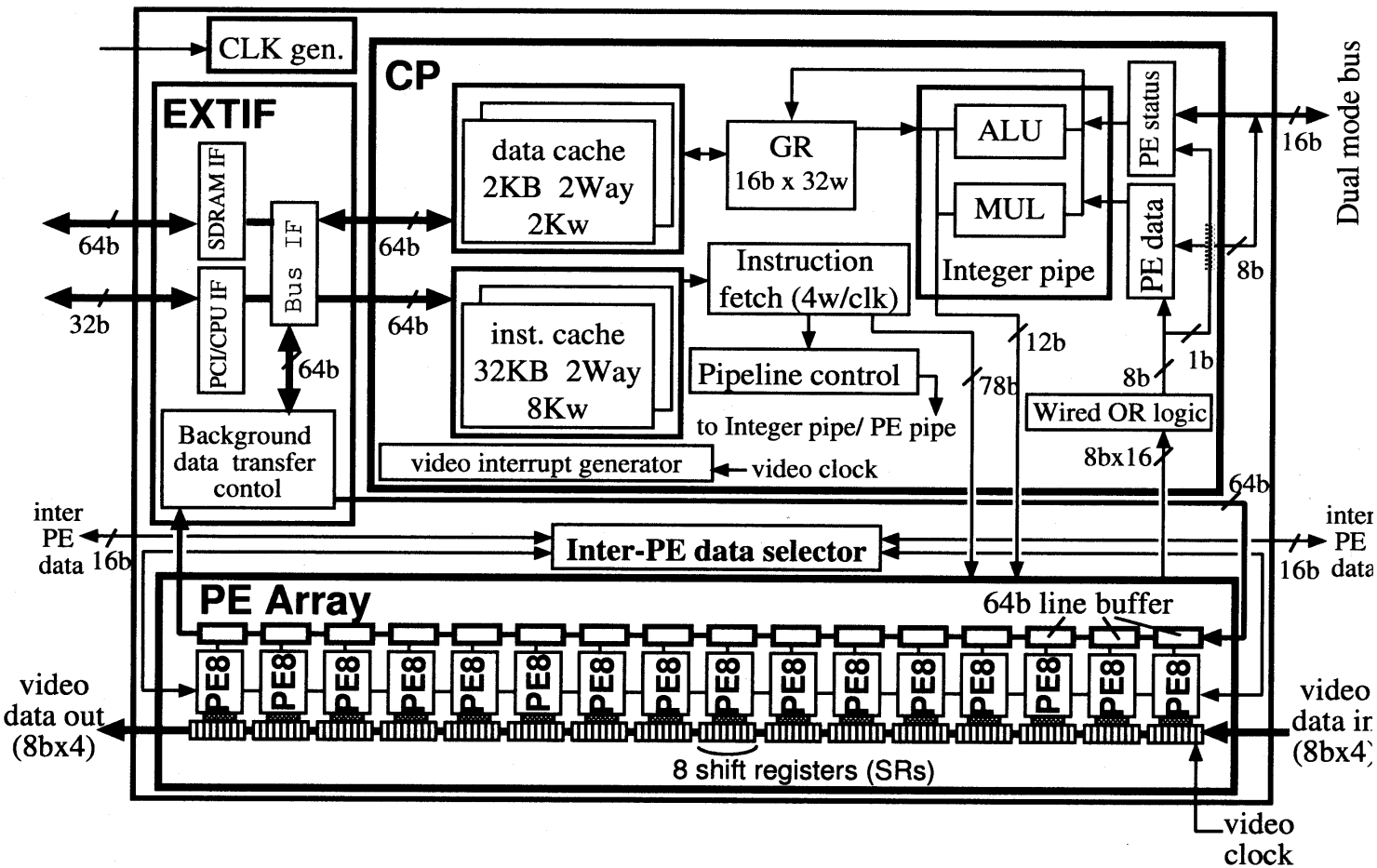
IMAP - Programming Model

- *One-Dimensional C* (1DC)
- C programming language with data-parallel extensions
  - Description of data structures spread across IMEM
  - SIMD processing of these structures
  - Collection of results
- Main code runs on the CPU; 1DC compiler automatically dispatches parallel operations to the PEs

IMAP-CE

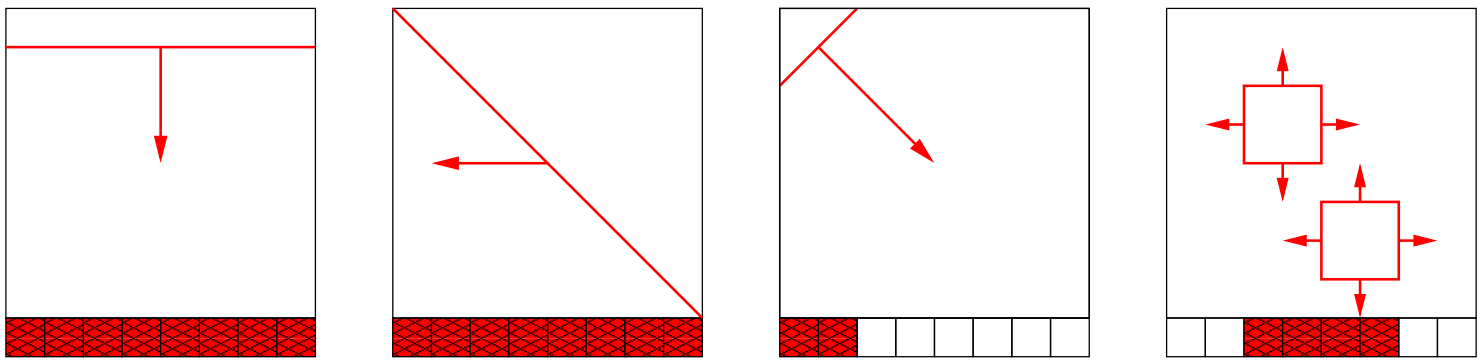
- Prototype IMAP implementation, developed by Kyo et al.
- CPU is now integrated onto the chip as the *Central Processor* (CP)
- 128 PEs, 2KB of IMEM each
  - Designed to hold an entire 512x512 image in PE IMEM

IMAP-CE - Internal Design



IMAP-CE - Usage

- Builtin support for four types of image access
  (a) Row-wise
  (b) Row-systolic
  (c) Slant-systolic
  (d) Autonomous



IMAPCAR

- Refinement of IMAP-CE, designed for use in automobiles
- ROI and DMA upgrades, including ROI scaling
- Video bus width tripled; IMAPCAR can handle two 768p or three 512p video streams simultaneously
- Program and data memory protected by ECC and parity checks respectively

ROI	Region of Interest
DMA	Direct Memory Access
ECC	Error Correction Code

IMAPCAR In Practice

- Benchmarks:
  - 3x faster than IMAP-CE
  - Comparable power requirements

IMAPCAR - Weaknesses

- Initial stages of image analysis are all SIMD
- Once regions of interest are identified, they must be analyzed
- Analysis is intrinsically MIMD
- Problem: IMAPCAR has no MIMD support!
- ROI analysis ends up happening in serial on the CP, with the PEs idle

IMAPCAR - Possible Solutions

- Use multiple IMAPCAR chips
  - Cost and power draw increase proportionally
  - Extra IMAPCARs are idle when performing SIMD operations
  - All PEs are idle when performing MIMD operations
- Add more CPs to the IMAPCAR
  - Greatly increases complexity
  - Still "wastes" the PEs

IMAPCAR2

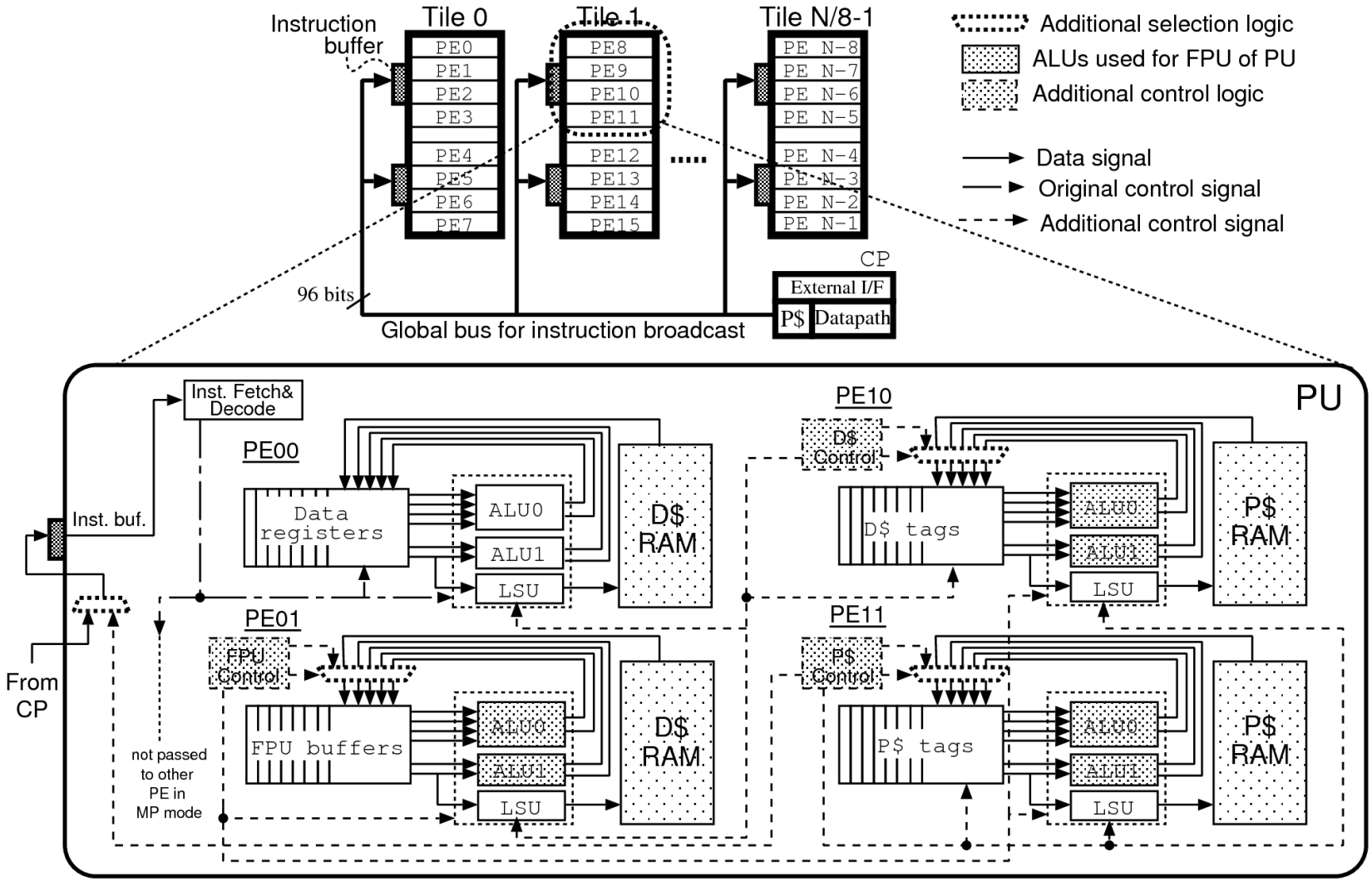
- Successor to IMAPCAR, intended to address MIMD issue
- Minor upgrades:
  - PEs and CP now use the same datapath and instruction set
  - IMEM amount doubled
  - Tiling capability
  - 16-bit addressing and instruction width

IMAPCAR2 - MIMD Support

- PEs are grouped into sets of 4
- Each group is augmented with hardware that lets them combine to function as an additional CP
  - IMEM becomes data and instruction caches
  - Extra ALUs become FPU components
  - PE 0 handles registers and instruction dispatch
- Total hardware overhead is around 20%

ALU	Arithmetic/Logic Unit
FPU	Floating Point Unit

IMAPCAR2 - Internal Design



IMAPCAR2 - Programming Model

- Like earlier IMAPs, uses 1DC
- Additional extensions for controlling PUs
- C API for PU usage is pthreads-compatible, ie, shared-memory
  - Synchronization via shared structures - mutexes, semaphores, barriers
  - Communication by reading and writing known areas of memory

IMAPCAR2 - Weaknesses

- Pthreads-alike programming model implies shared memory
- However, the IMAPCAR2 has no cache coherency
  - Cache$\leftrightarrow$RAM transfers must be explicitly invoked
- Trying to use IMAPCAR2 as a shared-memory system will not work
- Unlike IMAPCAR's deficiencies, this can be fixed entirely in software by providing a message-passing API

Conclusions

- IMAP is an old but still highly effective architecture for image processing
- IMAPCAR2 shows promise as a modern refinement of that design
- However, additional software support is needed to fully realize its potential

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